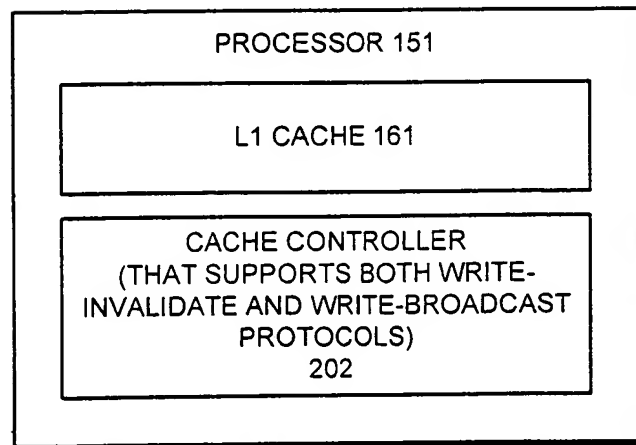
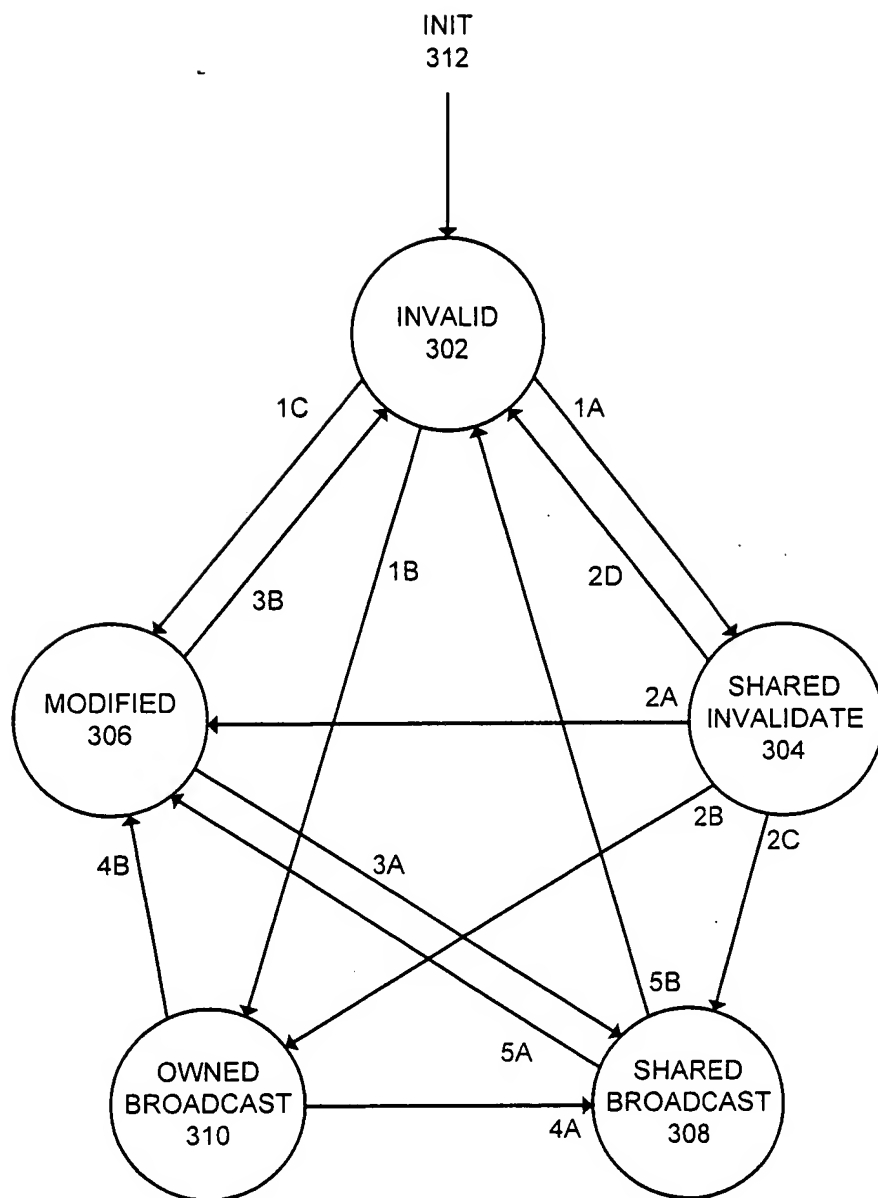


**FIG. 1**  
(PRIOR ART)



**FIG. 2**



**FIG. 3A**

TRANSITION	CPU ACTION	SNOOP RESP.	BUS ACTION	OBSV. ACTION
1A	READ	MEMORY	RTS	
1B	READ/WRITE	CACHE INTRV.	RTS/RTO+WBC	UPDATE
1C	WRITE	MEMORY	RTO	
2A	WRITE	NOSHARE	RTO	
2B	WRITE	SHARE	WBC	UPDATE
2C	N/A	N/A	FOREIGN WBC	UPDATE
2D	CAST OUT	N/A	N/A	
3A	N/A	N/A	FOREIGN RTS/RTO	
3B	CAST OUT	N/A	INV	INVALIDATE
4A	N/A	N/A	FOREIGN RTS/RTO	
4B	WRITE>MAX	DON'T CARE	INV	INVALIDATE
5A	WRITE>MAX	DON'T CARE	INV	INVALIDATE
5B	CAST OUT	N/A	WBC	

**FIG. 3B**